Application No.: 09/893,559 2 Docket No.: 8733.448.00-US

REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the subject application. The Non-Final Office Action of February 24, 2004 has been received and its contents carefully reviewed.

In the Office Action, the Examiner rejected claims 1-11 under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention; claims 12-18 and 24 under 35 U.S.C. § 102(e) as anticipated by Great Britain Patent No. GB 2344840 to Kim ("Kim"); claims 12-17 under 35 U.S.C. § 102(b) as anticipated by Japanese Patent No. 9270936 to Akira ("Akira"); claims 30 and 33 under 35 U.S.C. § 102(e) as anticipated by U.S Patent No. 6,329,975 to Yamaguchi ("Yamaguchi"); and 19-23, 25-29, 31, 32, 34, and 35 under 35 U.S.C. § 103(a) as being unpatentable over Kim.

In rejecting claims 1-11 under 35 U.S.C. § 112, first paragraph, the Examiner requested support for the phrase "counting a number of contiguous non-alternating states." Counting a number of non-alternating states, is carried out by the frequency comparator 44 and the signal presence comparator 48 when it determines the frequency difference as indicated by the intermediate signal. (See Fig. 4, and page 9, li. 26 to page 10, li. 20.) The frequency comparator 44 produces an intermediate signal with a frequency indicating the difference in frequency between the input signal 42 and the pre-synchronizing signal 41. When there is no or a very small frequency difference between the input signal 42 and the pre-synchronizing signal 41, the intermediate signal has no frequency, that is, the intermediate signal has a constant value. The signal presence comparator is looking for an intermediate signal with this characteristic. This is done by looking at contiguous states or periods of the intermediate signal. When contiguous

states do not have alternating values, as would be the case when the intermediate signal has a small frequency value, these states are counted over time. When a certain number of states or periods are counted that are non-alternating, then the signal presence comparator determines that there is a signal present because the intermediate signal has a small frequency indicating that the input signal has a frequency near the pre-synchronizing signal. In light of the above identified support in the specification for the terms identified by the Examiner, the Applicant believes that the rejection under 34 U.S.C. § 112, first paragraph, is overcome.

The Applicant appreciates the Examiner's courtesy extended during a phone conversation on April 7, 2004 regarding the rejection of claims 12-18 and 24 under 35 U.S.C. § 102(e) as anticipated by Kim. During that conversation the Examiner stated that Kim should be applied under 35 U.S.C. § 102(a) instead of 35 U.S.C. § 102(e). The publication date of Kim is May 2, 2001. The present application was filed on June 29, 2001 and claims priority to Korean Patent Application No. 2000-76850 filed December 15, 2000. The Applicant submits herewith a certified translation of Korean Patent Application No. 2000-76850 to perfect the priority claim. Therefore, Kim is not available as a reference, and the Applicant respectfully requests the Examiner to remove this rejection and allow claims 12-18 and 24.

The rejection of claims 12-17 under 35 U.S.C. § 102(b) as anticipated by Akira is respectfully traversed and reconsideration is requested. Claim 12 is allowable over the cited reference in that claim 12 recites a combination of elements including, for example "outputting a signal of a first state if the first period is less than the first reference period". Claim 14 is allowable over the cited reference in that claim 12 recites a combination of elements including, for example "outputting a signal of a first state if the first period is greater than the first reference period". Claim 16 is allowable over the cited reference in that claim 12 recites a combination of elements including, for example "outputting a signal of a first state if the first period is less than

the first reference period and greater than the second reference period". Akira does not teach or suggest at least these features of the claimed invention.

Akira is directed to a synchronization detector circuit for a plasma display panel that reduces power consumption. Specifically, detector circuit in Akira separates out a horizontal synchronizing signal from the a video signal, which may be a NTSC or PAL/SECAM video signal having different horizontal synchronization frequencies. The frequency of the separated horizontal synchronizing signal is compared to a reference signal from one of two oscillators. One oscillator produces a signal with a NTSC horizontal synchronizing signal frequency, and the second oscillator produces a signal with a PAL/SECAM horizontal synchronizing signal frequency. The synchronization detection section 2 outputs a "signal representing the synchronization state only when the frequency of the oscillation signal output from an oscillator and frequency of the horizontal synchronizing signals are the same." If they are the same a changeover control section 7 keeps a switch 5 in position. If the synchronization detection section 2 does not output a signal, then the changeover control section 7 causes the switch to change and connect the other oscillator to the synchronization detection section 2. Therefore, Akira only outputs a signal state when the frequencies or periods are the same. When the periods are not the same the synchronization detection section 2 does output a signal. Claims 12, 14, and 16 include outputting a signal when the periods are different as described above and, therefore, are allowable over Akira. Accordingly, Applicants respectfully submit that claims 13, 15, and 17, which depend from claims 12, 14, and 16 respectively, are also allowable over the cited references.

The rejection of claims 30 and 33 under 35 U.S.C. § 102(b) as anticipated by Yamaguchi is respectfully traversed and reconsideration is requested. Claim 30 is allowable over the cited reference in that claim 30 recites a combination of elements including, for example "a period

detector for comparing a data enable signal from the exterior thereof with the reference clock to output a period of the input signal with the aid of a detection reference signal and the presynchronizing signal" and "a period comparator for comparing a period range between a desired maximum value and a desired minimum value of the input signal." Claim 33 is allowable over the cited reference in that claim 33 recites a combination of elements including, for example "comparing a data enable signal from the exterior with the reference clock to output a period of the input signal with the aid of a detection reference signal and the pre-synchronizing signal" and "comparing a period range between a desired maximum value and a desired minimum value of the input signal." Yamaguchi does not teach or suggest at least these features of the claimed invention.

Yamaguchi is directed to a providing an output signal to a display whether or not a data enable signal is available. If a data enable signal is available Yamaguchi displays the image received using the received H_{sync} and V_{sync} signals. (See Fig. 3 and col. 4, ll. 42-5.) If the data enable signal is not available, Yamaguchi displays the image received using H_{spl} and V_{spl} generated by a start pulse generation circuit 7. (See col. 5, ll. 9-16.) In the Office Action, the Examiner states: "SEE column 4, lines 45-55; 'if the data enable signal indicating the effective display data **period is** not **detected** for more than a constant period, a select signal is generated. For example, if the data enable signal indicating an effective display period is not detected for a **specific length** of time or longer' note this reads on minimum to maximum." Yamaguchi is determining whether a data enable signal is present or not by looking for a data enable signal over a constant or specific length of time. If the data enable signal is detected during the specified length of time it is present, if not it is assumed that it is not present. This is determining whether the period is greater than a specific time. The present invention determines if the period is within a range defined by a desired minimum and maximum value. Yamaguchi

does not compare a period range as recited in claims 30 and 33 above. Further, the Examiner identifies the data enable signal detection circuit 11 of Yamaguchi as the period detector. The data enable signal detection circuit 11 receives the data enable signal and the V_{sync} signal. (See col. 4, ll. 42-45.) In the claimed invention, the data enable signal is compared to the reference clock that has the same frequency as the horizontal synchronizing signal, and not to a vertical synchronizing signal. Therefore, claims 30 and 33 are allowable over Yamaguchi.

The rejection of claims 19-23, 25-29, 31, 32, 34, and 35 under 35 U.S.C. § 103(a) as being unpatentable over Kim is now moot in light of the perfection of a claim for priority as discussed above that removes Kim as a prior art reference. Therefore, the Applicant respectfully requests the Examiner to remove this rejection and allow claims 19-23, 25-29, 31, 32, 34, and 35.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Docket No.: 8733.448.00-US

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. § 1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Dated: Mey 18, 2004

Respectfully submitted,

Registration No.: 40,106

MCKENNA LONG & ALDRIDGE LLP

1900 K Street, N.W. Washington, DC 20006

(202) 496-7500

Attorney for Applicant